GE Fanuc
Intelligent Platforms

Technical Needs and Challenges in Harbor Surveillance

Introduction

Sonar for naval applications was originally developed to detect and locate underwater threats in deep water, such as submarines. It was discovered that this deep water sonar was not very effective at locating smaller objects such as mines. It became well known that in order to detect and localize small objects in the water, higher sonar frequencies were required. The use of these higher frequencies added significant complexity to the systems required to acquire and analyze the sonar data.

The hardware used to build such systems has changed considerably over the last ten years. A large percentage of current generation data acquisition hardware available in the market today utilizes FPGAs due to their flexibility of use and their inherent ability to manage data. By taking advantage of the additional data processing capability available within these FPGAs, unique solutions can be offered to integrators of high frequency sonar systems which can lower the overall system cost and simplify system design.

This paper will look at traditional solutions to the implementation of a high frequency sonar system and compare them to one of the simpler solutions available with modern FPGA enabled hardware offerings. This comparison is especially relevant today since the requirement to detect small items in the water has expanded from just mines to include such diverse objects such as divers, swimmers, and small water vehicles all in the interest of harbor security and coastal defense.

Comparison of Hardware Solutions

We can illustrate the added complexity of high frequency sonar through a comparison of the hardware required to create a low-frequency sonar system and a high-frequency sonar system. A sonar system consists of many different components – hardware such as transducers, amplifiers, switches, signal conditioning, signal acquisition, and data processing elements including beamforming, tracking, and classification. Our comparison will look at the hardware required for the signal conditioning through to the beam-formed data. For comparison purposes, we will consider the hardware available from GE Fanuc Intelligent Platforms.

Example One: Deep water sonar (low frequency)

Let's look at a set of operating parameters that are typical for a deep water sonar system:

Sampling Frequency (Fs):	12.5 kHz
Bandwidth:	5 kHz
Number of beams (NB):	32
Number of hydrophones (NH):	96

As can be seen from the block diagram, we would need three ICS-110B1L-32 cards to filter, amplify, and digitize the incoming hydrophone data, and two ICS-2200B cards to calculate the real time beam data.

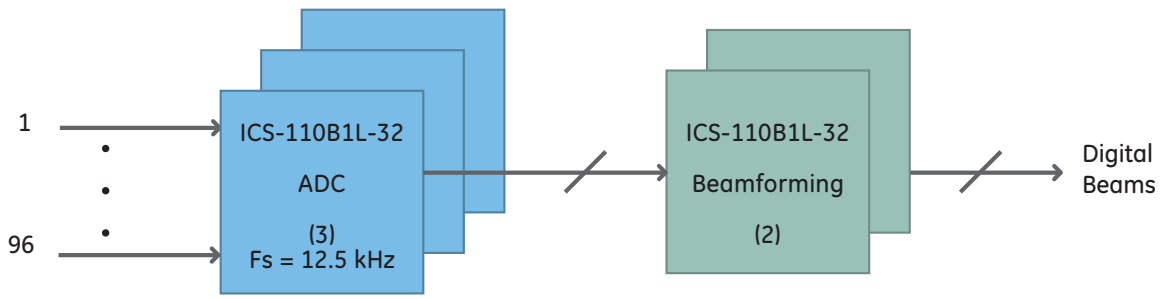

Figure 1. Block Diagram of Low Frequency Sonar SubSystem

Processing required for beamforming:

Assume time domain beamforming with 4 tap interpolation (NT).

Shading requires NH*Fs multiplications per second

Interpolation requires NH*NT*NB*Fs multiplications per second and NH*(NT-1)*NB*Fs additions per second

Entering the numbers summarized above: 21,600*Fs, or 270 million mathematical operations per second

It's easy to see from this formula that the amount of processing involved is proportional to the sampling frequency. The actual formula which represents the number of beams per ICS-2200B card is:

$$NB = \frac{\frac{40E6}{Fs} - \frac{NH}{2} - 48}{\frac{NH * NT}{2}}$$

List price for example one: $121,000

Example Two: High Frequency sonar

Let's look at a similar set of operating parameters that are typical for a high frequency sonar system:

Sampling Frequency (Fs): 75 kHz

Bandwidth: 30 kHz

Number of beams (NB): 32

Number of hydrophones (NH): 96

As can be seen from the block diagram, we would need the same number of ICS-110B1L-32 cards to filter, amplify, and digitize the incoming hydrophone data, and 16 ICS-2200B cards to calculate the real time beam data. Since the processing does not scale entirely linearly with sampling frequency (due to the architecture of the ICS-2200B card), we need more than 6 times the number of processing cards (75 kHz is six times higher than 12.5 kHz).

List price for example two: $366,000

As can be seen in example two, the amount of hardware and the subsequent cost goes up substantially with a higher sampling rate. One of the techniques commonly used to combat this is to demodulate the band of interest prior to beamforming. This technique is possible since the signal to be received is typically the reflected echo of a bandlimited transmit signal (or ping). Demodulation lowers the data rate to the beamformer, by translating the band of interest down to baseband, thus reducing the amount of beamforming hardware required. Let's continue our architecture comparison by reconfiguring example two to use complex demodulation prior to beamforming.

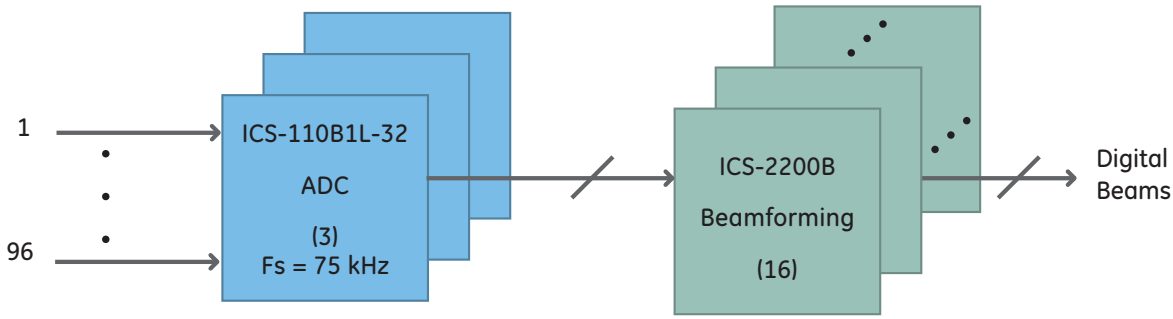

Figure 2. Block Diagram of Full-band High Frequency Sonar SubSystem

Example Three: High Frequency sonar using Complex Demodulation

We start with the same operating parameters as in Example Two, along with additional information, the bandwidth and centre frequency of the signal of interest.

Sampling Frequency (Fs):	75 kHz
Number of beams (NB):	32
Number of hydrophones (NH):	96
Bandwidth (bw):	10 kHz
Centre Frequency (Fc):	25 kHz

We need to add an initial stage of complex demodulation prior to beamforming. If we assume a decimation of 6, giving an output data rate of 12.5 kHz, we have a transition band (TB) of 1.25 kHz at each edge of the band of interest (transition band refers to the edges of our band of interest where digital filtering must reduce the signal energy sufficiently to avoid aliasing when the digital signal is decimated). A general rule of thumb is that the number of taps required for the digital filter is 2*Fs/TB, which in this case gives us 120 taps. This can be accomplished with four ICS-2200 cards.

By reducing the sample rate from 75 kHz down to 12.5 kHz, we can reduce the number of ICS-2200 cards required to perform beamforming down from 16 to 6, for a net reduction of 6 cards.

List price for Example Three: $261,000

Example Four: High Frequency Sonar using MDACs
Adding complex demodulation prior to beamforming gives a significant cost reduction. Another approach that had been developed with the same desire to reduce the amount of processing hardware required was to use MDACs prior to the digitization process (see block diagram in Figure 4). An MDAC is a D/A converter that multiplies an analog input signal, applied at a reference input, by the value applied to the digital inputs. In this case, the transducer signal is applied to the reference input and the digitized mixing (IF) waveform to the digital input. The input signal is therefore scaled (or multiplied) by the IF. For quadrature demodulation two MDACs are required, one for the cosine and the other for sine data. Since the data is applied digitally, the IF is programmable. Since sigma-delta analog to digital converters use over-sampling and a very steep digital filter, the signals that are aliased due to the mixing process are automatically filtered out.

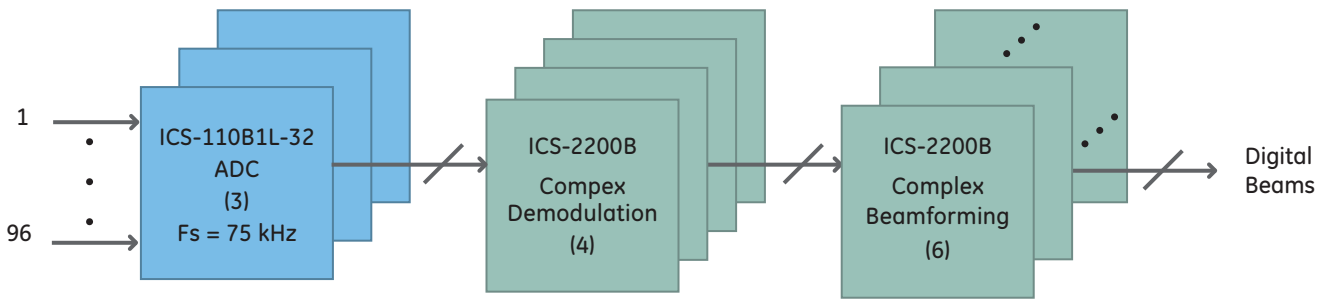

Figure 3. Block Diagram of Band Selective High Frequency Sonar SubSystem

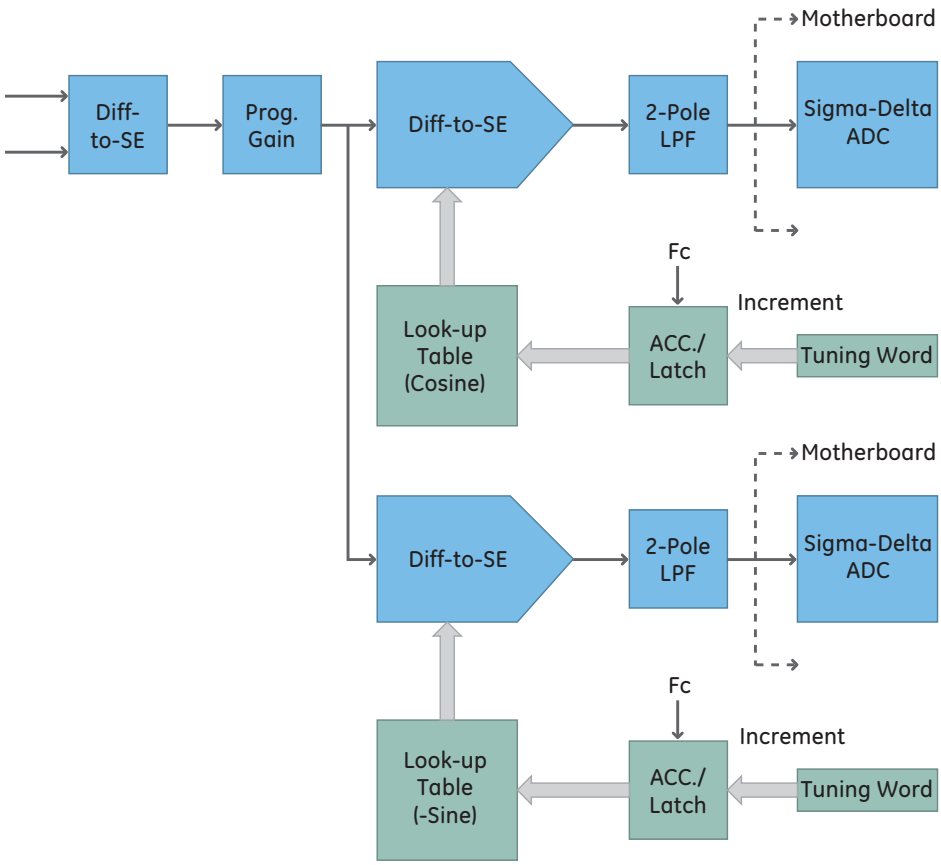

Figure 4. ICS-110B2L Daughter Card Block Diagram (One Channel)

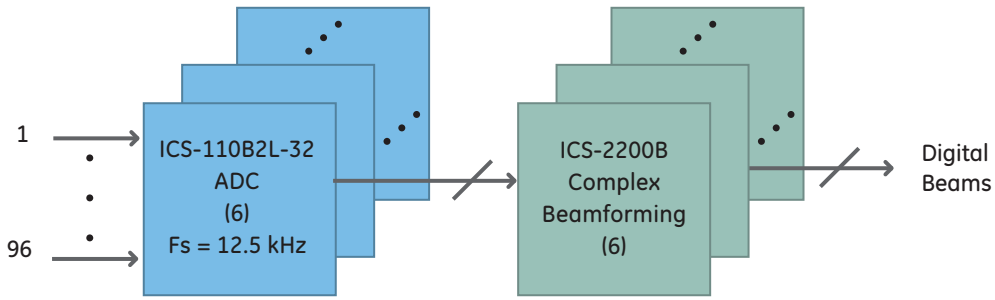

Figure 5. Block Diagram of High Frequency Sonar SubSystem Using MDAC Approach

As can be seen from the block diagram, twice as many digitization cards are required since the MDAC process creates twice as many analog signals (representing I&Q complex signals). One additional note of interest on this approach is that additional post processing is required to remove the difference in the DC offset between the two ADCs that are used per channel. The mismatch in DC offset has the effect of creating a tone in the center of the frequency band.

Cost for Example Four: $255,000

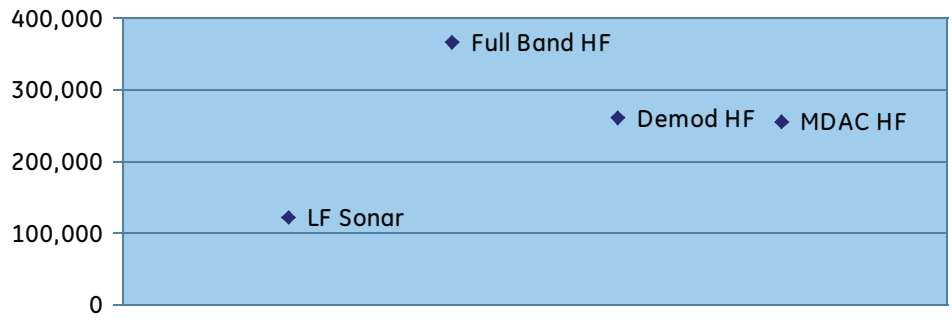

Figure 6. Cost Comparison of Traditional Approaches

New Approach Using Acquisition Server Concept

The previous four examples have illustrated the options available to systems integrators in the past ten years. The latest generation of acoustic acquisition hardware available from GE Fanuc Intelligent Platforms has opened up new possibilities by taking advantage of embedded FPGA resources available that are currently being used to handle data flow management.

It is common to find FPGA's in the design of data acquisition hardware. Often times these FPGA's are used in order to take advantage of their inherent data handling capabilities. For example, FPGA's can be used to convert a parallel data bus coming from an analog to digital converter into a high speed serial data stream (or vice versa). This often leaves untapped data processing capabilities available in the on-board hardware.

The daqNet, introduced by GE Fanuc Intelligent Platforms in 2007, represents a new concept in data acquisition by providing a box level solution with a control and data flow path through Ethernet. daqNet provides better signal performance, higher channel density, and easier integration, all at a lower cost per channel than comparative board level solutions. The design of the daqNet was accomplished with an FPGA module on each style of I/O module to facilitate the high speed data flow through to the embedded controller. By taking advantage of the processing capability of this FPGA, it is possible to implement a complex demodulation core, which not only reduces the beamforming processing required, but also reduces the data flow through the Gbit Ethernet interface.

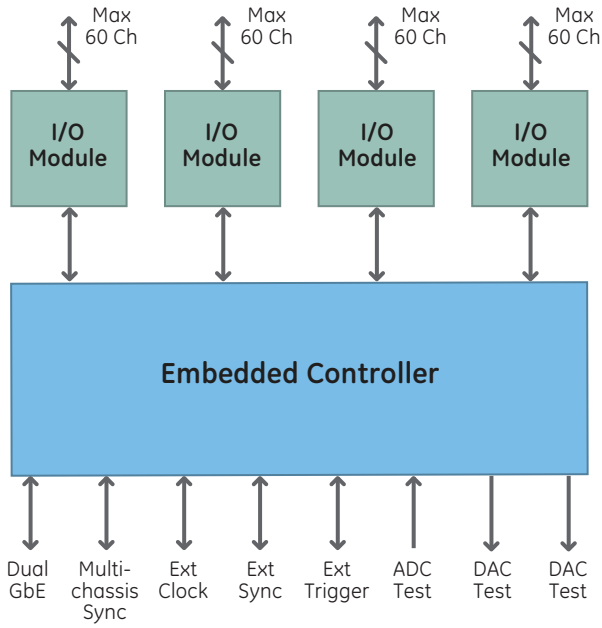

Figure 7. Block Diagram of daqNet Acoustic Acquisition Server

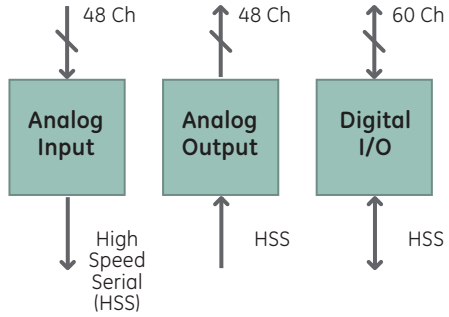

Figure 8. Available I/O modules

Cost of daqNet based solution (pre-beamforming): $50,000

As this cost doesn't include beamforming, we must compare it to the pre-beamforming costs of examples three ($156,000), and four ($150,000). As can be seen, there is a significant cost benefit to using the latest generation of data acquisition hardware along with embedded processing (not to mention a significant savings in rack space). This is further supported by the fact that current Intel processors are often capable of performing the beamforming operation leading to a further reduction in the overall high frequency sonar cost.

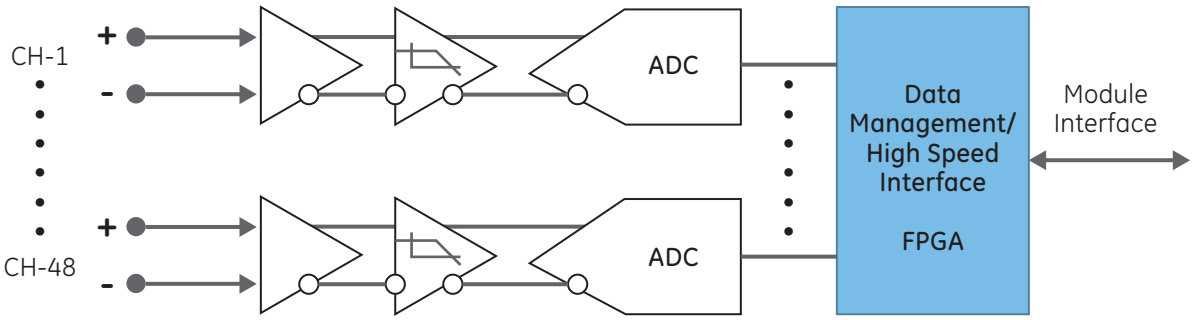

Figure 9. Detail of Analog Input (AI) Module

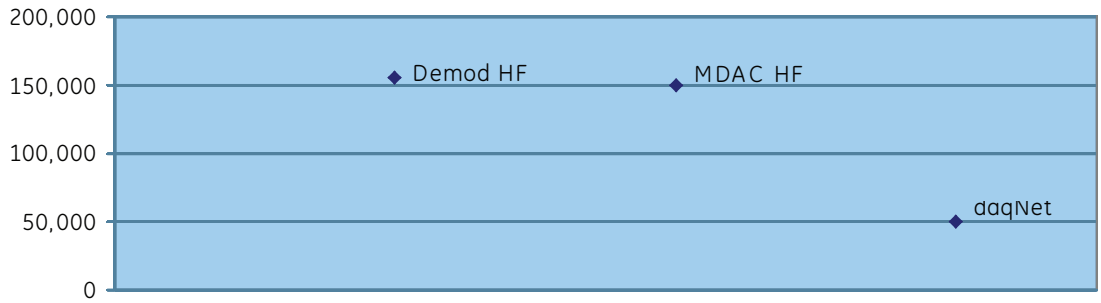

Figure 10 – Cost Comparison of Pre-Beamforming Solutions

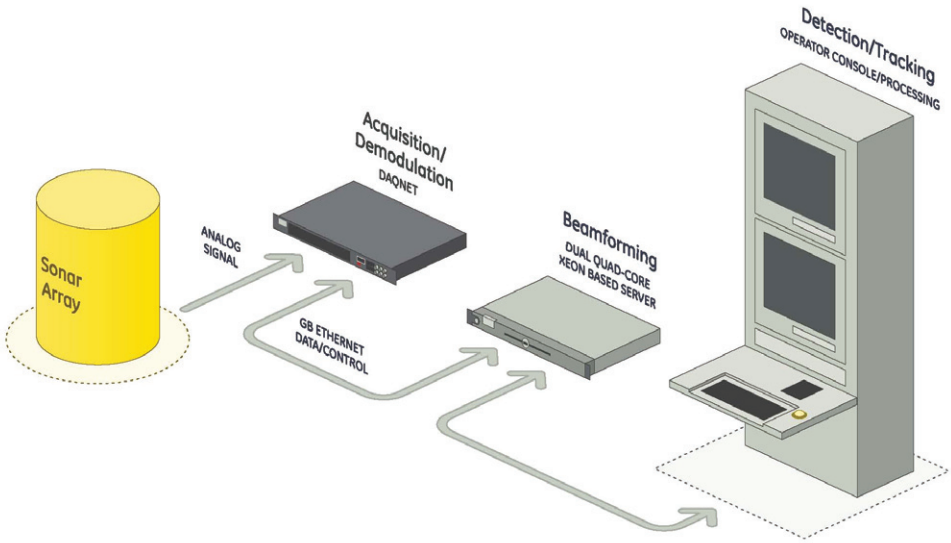

Figure 11. daqNet – Sonar Implementation

Conclusion

FPGA based data processing continues to change the landscape of data acquisition. By taking advantage of the data processing capabilities available in FPGA's which are added to hardware designs to handle data movement, significant cost reductions can be introduced into complex systems, such as high frequency sonar systems. This allows integrators of harbor surveillance and coastal defense systems to accomplish more with less.

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Additional Resources

For more information, please visit the GE Fanuc Intelligent Platforms web site at:

www.gefanuc.com

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